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09/213,748	12/17/1998	EDWARD G. CALLWAY	0100.01319	6443

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EXAMINER	
HARRISON, CHANTE E	

ART UNIT	PAPER NUMBER
2672	24

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/213,748	Applicant(s) CALLWAY ET AL.	
	Examiner Chante Harrison	Art Unit 2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *07 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4 and 6-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *31-37* is/are allowed.

6)☒ Claim(s) *2-4,6-11,14-23,26-30 and 38* is/are rejected.

7)☒ Claim(s) *12-13,24-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communications: Amendment D, filed on 6/7/04.

T***his action is made FINAL.***

2. Claims 2-38 are pending in the case. Claims 4, 20, 30, 31 and 38 are independent claims. Claims 31-37 are indicated as being allowable over the prior art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4, 6-11, 14-23, 26-30 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto, U.S. Patent 5,912,710, 6/1999 and further in view of Allen Porter, U.S. Patent 6,208,354, 3/2001.

As per independent claim 4, Fujimoto discloses a video scaler to receive and scale video based on a ratio between the input format and the output format (FIG. 1 "107"), a graphics scaler to receive and scale graphics based on a ratio between the input format and the output format (FIG. 1 "106"), combining the video and graphics to produce video graphics output (FIG. 1 "108"; FIG. 6; FIG. 8 "203"), a first memory (FIG.

1 "100g") having graphics data and a second memory (FIG. 1 "100b") having video data and the two memories coupled to their corresponding scalers (FIG.1). Fujimoto fails to disclose a single frame buffer memory, which Porter discloses (col. 2, ll. 40-55). Fujimoto teaches storing the separate video and graphics data together on media accessible by main memory, which individually retrieves both graphics and video data and forwards the individual data through respective processing channels to be scaled (FIG. 1; col. 11, ll. 15 et seq.). Porter teaches a video graphics circuit for retrieving, blending graphics and video data that is allocated to a frame buffer based on resolution (Fig. 1; col. 3, ll. 1-8), where the memory may be a DVD memory. It would have been obvious to one of skill in the art to include Porter's teaching of a single frame buffer memory in the disclosure of Fujimoto because Fujimoto provides memory read and write transactions from the CPU (col. 10, ll. 47-57), as does a frame buffer, whereas Porter's provision for memory allows for a single memory device that preferably a frame buffer that may be substituted for a DVD memory.

As per dependent claim 3, Fujimoto in view of Porter discloses the merging block receiving control data used to produce the video graphics output (FIG. 8 "201 & 203").

As per dependent claim 5, Fujimoto fails to disclose the first and second memory blocks included in a frame buffer of a video graphics integrated circuit, which Porter discloses (Fig. 1; col. 2, ll. 40-55).

As per dependent claim 6, Fujimoto in view of Porter discloses a video controller coupled to the video scaler (FIG. 1), a graphics controller coupled to the graphics scaler (FIG. 1) and the video and data controller are synchronized (FIG. 1; col. 10-11, ll. 60 et seq.).

As per dependent claim 7, Fujimoto in view of Porter discloses an alpha blend operation (FIG. 1 "108").

As per dependent claim 8, Fujimoto in view of Porter discloses a digital to analog converter for the video graphics (col. 10, ll. 35 et seq.).

As per dependent claim 9, Fujimoto in view of Porter discloses a display driver (FIG. 18 "18c") formatting the output (col. 6, ll. 40 et seq.; col. 10, ll. 10-25, 60 et seq.).

As per dependent claim 10, Fujimoto in view of Porter discloses a driver coupled to a video scaler (FIG. 18 "18c").

As per dependent claim 11, Fujimoto in view of Porter discloses a driver coupled to a graphics scaler (FIG. 18 "18c").

As per dependent claim 14, Fujimoto in view of Porter discloses a plurality of graphics scalers (Fig. 19).

As per dependent claim 15, Fujimoto in view of Porter discloses the merging block configuring a pixel rate of the video output stream to produce a preferred video scaling ratio (col. 2, ll. 46-64; col. 3, ll. 18-35).

As per dependent claim 16, Fujimoto in view of Porter discloses the merging block configuring a pixel rate of the video output stream to produce a preferred graphics scaling ratio (col. 2, ll. 46-64; col. 3, ll. 18-35).

As per dependent claim 17, Fujimoto in view of Porter discloses a video decompression block (FIG. 1 "102").

As per dependent claim 18, Fujimoto in view of Porter discloses a graphics decompression block (FIGS. 1 & 17; col. 15, ll. 10 et seq.).

As per dependent claim 19, Fujimoto in view of Porter discloses the video stream is a decoded MPEG data stream (FIG.1 "102").

As per independent claim 20, Fujimoto discloses a video scaler to receive and scale video based on a ratio between the input format and the output format (FIG. 1 "107"), a graphics scaler to receive and scale graphics based on a ratio between the input format and the output format (FIG. 1 "106"), combining the video and graphics to

produce video graphics output (FIG. 1 "108"; FIG. 6; FIG. 8 "203"), allocating a first block of memory for storing the video data stream (FIG. 1 '100B'), allocating a second block of memory for storing the graphics data stream (FIG. 1 '100G'). Fujimoto fails to specifically disclose allocating memory in a frame buffer based upon memory needs of the data stream. Porter teaches allocating memory in a frame buffer based upon needs of the data stream (col. 2, ll. 40-55; col. 3, ll. 1-8). Fujimoto teaches a CPU controlling operation of a DVD that provides video and graphics data to a system that performs an operation on the data as defined by the application program and outputs the data for display (Fig. 1). Porter teaches a video graphics circuit for retrieving and blending data allocated to a frame buffer based on resolution (Fig. 1; col. 3, ll. 1-8), where the memory may be a DVD memory. It would have been obvious to one of skill in the art to include Porter's teaching of memory allocation in a frame buffer based upon need in the disclosure of Fujimoto because Fujimoto provides memory read and write transactions from the CPU (col. 10, ll. 47-57), as does a frame buffer, whereas Porter's provision for memory allows for a single memory device that preferably a frame buffer that may be substituted for a DVD memory.

As per dependent claims 2 and 21, Fujimoto discloses a controller (FIG. 8 "122") providing data to the video and graphics scalers (FIG. 8) and allocating memory to the first and second blocks of memory, but fails to specifically disclose allocating memory based upon memory needs of the data stream. Porter teaches allocating memory

based upon needs of the data stream (col. 3, ll. 1-8). Fujimoto teaches a CPU controlling operation of a DVD that provides video and graphics data to a system that performs an operation on the data as defined by the application program and outputs the data for display (Fig. 1). Porter teaches a video graphics circuit for retrieving and blending data allocated to a frame buffer based on resolution (Fig. 1; col. 3, ll. 1-8). It would have been obvious to one of skill in the art to include Porter's teaching of memory allocation based upon need in the disclosure of Fujimoto because Fujimoto provides memory read and write transactions from the CPU (col. 10, ll. 47-57), as does a frame buffer, whereas Porter's provision for memory allows for a single memory device that preferably a frame buffer that may be substituted for a DVD memory.

As per dependent claim 22, Fujimoto in view of Porter discloses the merging block receiving control data used to produce the video graphics output (FIG. 8 "201 & 203").

As per dependent claim 23, Fujimoto in view of Porter discloses a digital to analog converter for the video graphics (col. 10, ll. 35 et seq.).

As per dependent claim 26, Fujimoto in view of Porter discloses scaling the video based on a first format and a plurality of selected formats (FIG. 1 "107"; col. 6, ll. 45-48, 54-58).

As per dependent claim 27, Fujimoto in view of Porter discloses scaling the graphics based on a first format and a plurality of selected formats (FIG. 1 "106"; col. 6, ll. 45-48, 54-58).

As per dependent claim 28, Fujimoto in view of Porter discloses a video decompression block (FIG. 1 "102").

As per dependent claim 29, Fujimoto in view of Porter discloses a graphics decompression block (FIGS. 1 & 17; col. 15, ll. 10 et seq.).

As per independent claim 30, Fujimoto in view of Porter discloses a circuit (FIG.S. 1, 8 & 9) for implementing the method of claim 20. Therefore the rationale as applied in the rejection of independent claim 20 applies herein.

As per independent claim 38, Fujimoto in view of Porter discloses a system (Fig. 1) having memory maintaining video having a first format and graphics data having a second format (Fig. 1 "100"), but fails to disclose the memory allocated to the video and the graphics based on the needs of each. The rationale as applied to independent claim 20 applies herein.

Allowable Subject Matter

1. Claims 31-37 are allowed.

2. Claims 12, 13, 24 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

With respect to claims 4, 20, 30 and 38, Applicant argues combining the teachings of Fujimoto with that of Porter is improper as Fujimoto teaches three memory locations and Porter teaches a single memory location, where the memory has a physical location different from that of Fujimoto.

In reply, Applicant fails to specifically claim in what specific manner the memory is connected to other system components. Therefore, Fujimoto and Porter's disclosure of a memory connected to the system for performing in a manner similar to that claimed by Applicant is interpreted as a memory coupled to the system. Additionally, Fujimoto's discloses the loading the media (i.e. graphics and video) data from the DVD; where the graphics data is loaded into VRAM and the video data is loaded into main memory (col. 11, ll. 15-24). Fujimoto's disclosure fails to identify use of a frame buffer, which Porter

discloses (Fig. 1; col. 3, ll. 1-8). The combination of Fujimoto's disclosure in view of Porter is proper because Porter's suggests that a single memory device, such as a frame buffer, may be substituted for a DVD memory.

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chante Harrison whose telephone number is 703-305-3937. The examiner can normally be reached on Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Razavi can be reached on 703-305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chante Harrison
Examiner
Art Unit 2672

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JEFFERY BRIEN
PRIMARY EXAMINER